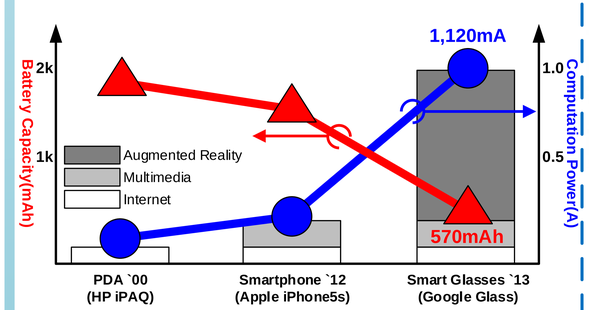
A Low-power and Real-time Augmented Reality Processor for the next generation Smart Glasses

Gyeonghoon Kim and Hoi-Jun Yoo, Korea Advanced Institute of Science and Technology (KAIST)

Hardware Requirements of Augmented Reality in Smart Glasses Systems

▣ Requirement #1: Low-Energy Consumption



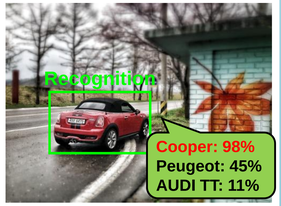
Hands-free Head Mounted Display (HMD)
- **Smaller Battery Size**
- **Complicated Markerless AR Functionalities**

▣ Requirement #2: High-Throughput Processing



Marker-based AR
- 2D-barcode / 2D-marker
- Markers on Everything?

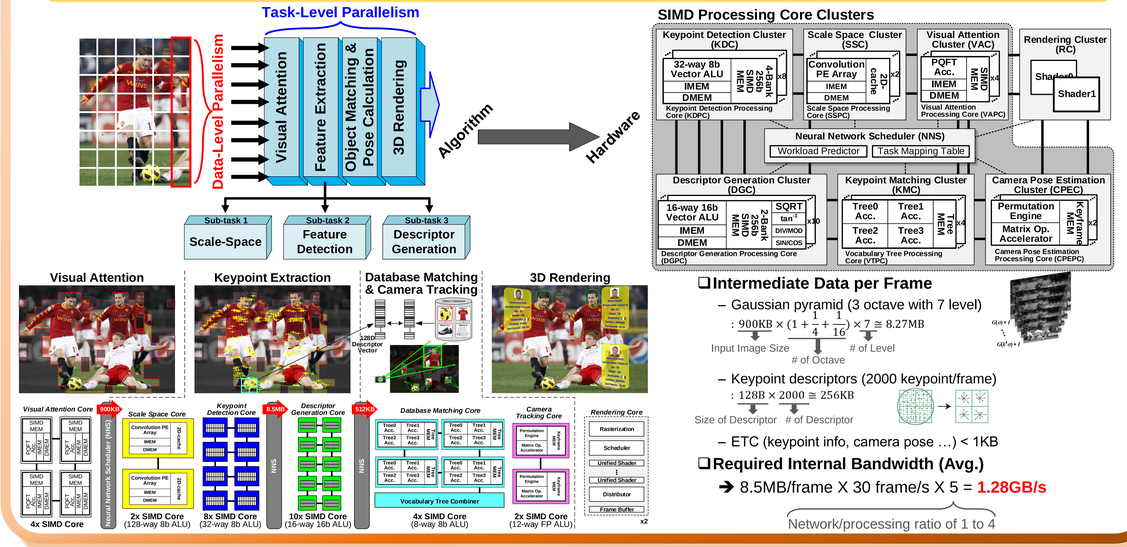
➔ **Impossible Solution in Real World**



Markerless AR
- Natural Feature Extraction
- >10x Higher Computation

➔ **Difficulties in Real-time (30fps) Operation**

Algorithm-Hardware Mapping and Network Congestion Problem



❑ **Intermediate Data per Frame**
- Gaussian pyramid (3 octave with 7 level)

$$\frac{900KB}{\text{Input Image Size}} \times \left(1+\frac{1}{4}+\frac{1}{16}\right) \times \underbrace{7}_{\#\text{ of Level}} \cong 8.27MB$$

(# of Octave)

- Keypoint descriptors (2000 keypoint/frame)

$$128B \times 2000 \cong 256KB$$

(Size of Descriptor × # of Descriptor)

- ETC (keypoint info, camera pose …) < 1KB

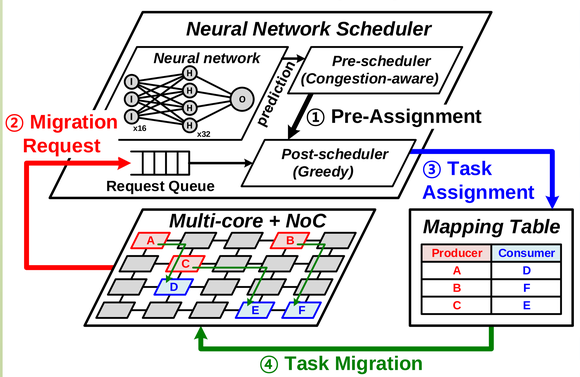
❑ **Required Internal Bandwidth (Avg.)**

➔ 8.5MB/frame X 30 frame/s X 5 = **1.28GB/s**

Network/processing ratio of 1 to 4

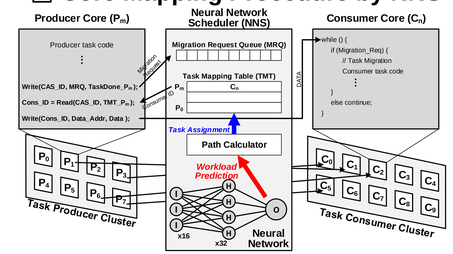
Neural Network Scheduler for 2D-mesh Network-on-Chip

▣ Overall Regulation Flow of Neural Network Scheduler (NNS)

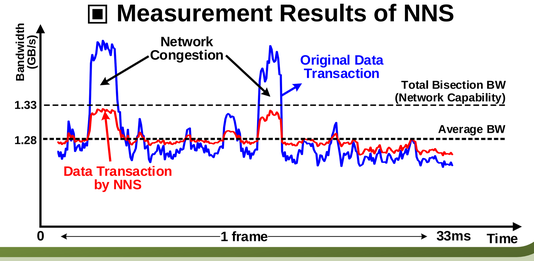


- Network Congestion Depends on Routing Path
- **Neural Network**: Workload Prediction
- **Mapping Scheduler**: Routing Path Decision

▣ Core Mapping Procedure by NNS

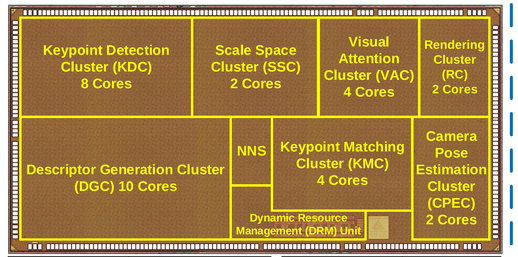


▣ Measurement Results of NNS



Chip and Smart Glass System Implementation Results

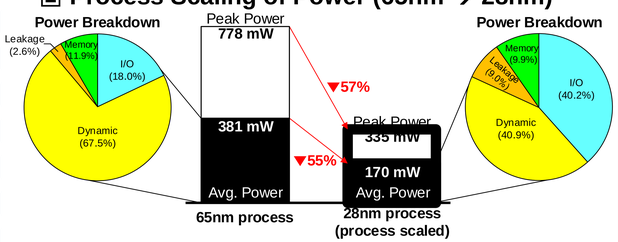
▣ Chip Implementation Results and Performance Summary



Technology	65 nm 1P8M Logic CMOS	
Chip Size	8.0 mm x 4.0 mm	
Supply Voltage	Nominal	1.2 V
	DVFS	0.7 ~ 1.2 V
Clock Frequency	Nominal	250 MHz (90FO4)
	DVFS	65 ~ 250 MHz
Power Consumption	Peak	778 mW
	Avg.	381 mW

Gate Count	8.32 M
SRAM	693 kB
Peak Performance	1.22 TOPS
Power Efficiency	1.57 TOPS/W
Area Efficiency	38.28 GOPS/mm²
Per-frame Energy	12.70 mJ/frame
Per-tile Energy	14.11 µJ/frame

▣ Process Scaling of Power (65nm → 28nm)



▣ Live Demonstration of Smart Glasses



E-mail: ghoon@kaist.ac.kr

KAIST

SSL Semiconductor System Lab.